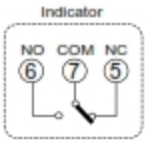
MC5, MC7

FAILSAFE



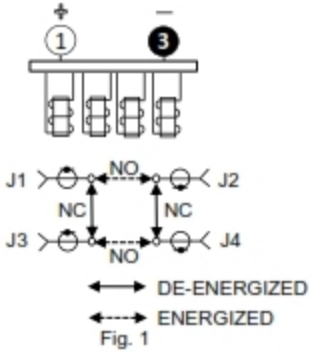


Fig. 1

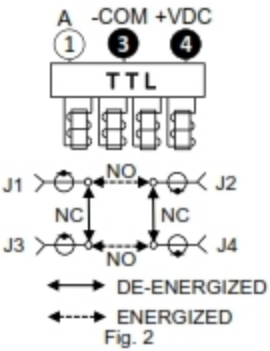
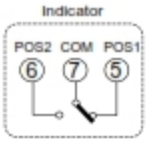


Fig. 2

LATCHING



PULSE

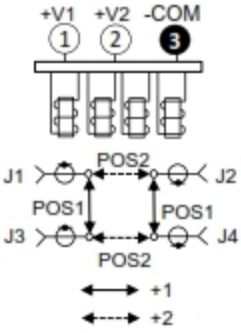


Fig. 3

TTL/SELF CUTOFF

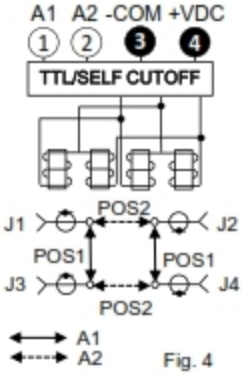


Fig. 4

SELF CUTOFF

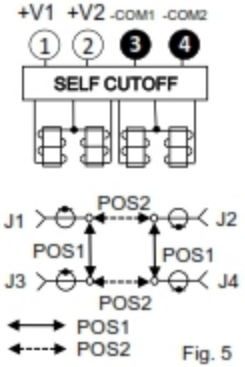


Fig. 5

LOGIC TRUTH TABLE

FAILSAFE (Figs. 1)

	RF PATH	+	-
POS1	J1-J3, J2-J4	0	GND
POS2	J1-J2, J3-J4	+VDC	GND

NOTE: +VDC=Positive rated voltage.

PULSE LATCHING (Fig. 3)

	RF PATH	+V1	+V2
POS1	J1-J3, J2-J4	+ΔV	0
POS2	J1-J2, J3-J4	0	+ΔV

NOTE: +ΔV=Positive rated voltage pulse.

FAILSAFE TTL (Figs. 2)

	RF PATH	A
POS1	J1-J3, J2-J4	0
POS2	J1-J2, J3-J4	1

LATCHING TTL/SELF CUTOFF (Fig. 4)

	RF PATH	A1	A2
POS1	J1-J3, J2-J4	1	0
POS2	J1-J2, J3-J4	0	1

LATCHING SELF CUTOFF (Fig. 5)

	RF PATH	IND PATH	+V1	+V2
POS1	J1-J3, J2-J4	IND1-C	+VDC	0
POS2	J1-J2, J3-J4	IND2-C	0	+VDC

NOTE: (1) TTL logic: low "0" = 0.0V – 0.8V; high "1" = 2.4V – 5.5V.
(2) "NC"=Normally Closed; "NO"=Normally Open.
(3) Consult the factory for the positive COM option.