MC3, MC6, MCH, MCJ, MCG, MCL

FAILSAFE / NORMALLY OPEN

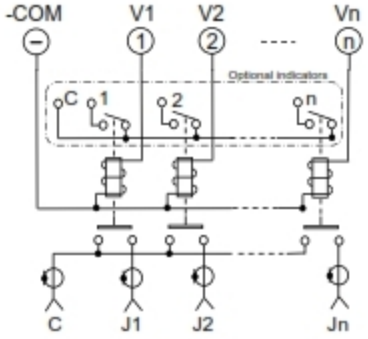

Fig. 1

FAILSAFE / NORMALLY OPEN with TTL

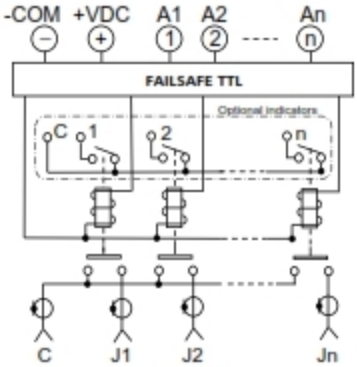

Fig. 2

LOGIC TRUTH TABLE

FAIL SAFE (Fig. 1)

RF PATH	V(n)	COM
J(n)-C	Rated +V	GND
J(n) Open	0	GND

FAIL SAFE with TTL (Fig. 2)

RF PATH	A(n)	+VDC	COM
J(n)-C	1	Rated +V	GND
J(n) Open	0	Rated +V	GND

NOTE: (1) TTL logic input A(n): low "0" = 0.0V – 0.8V; high "1" = 2.4V – 5.5V.

15-PIN D-SUB PINOUT	
Pin No.	PINOUT
1	V1 (J1-COM)
2	V2 (J2-COM)
3	V3 (J3-COM)
4	V4 (J4-COM)
5	V5 (J5-COM)
6	V6 (J6-COM)
7	V7 (J7-COM)
8	V8 (J8-COM)
9	V9 (J9-COM)
10	V10 (J10-COM)
11	V11 (J11-COM)
12	V12 (J12-COM)
13	COM(-)
14-15	UNUSED

15-PIN D-SUB PINOUT	
Pin No.	PINOUT
1	A1 (J1-COM)
2	A2 (J2-COM)
3	A3 (J3-COM)
4	A4 (J4-COM)
5	A5 (J5-COM)
6	A6 (J6-COM)
7	A7 (J7-COM)
8	A8 (J8-COM)
9	A9 (J9-COM)
10	A10 (J10-COM)
11	A11 (J11-COM)
12	A12 (J12-COM)
13	COM(-)
14-15	UNUSED