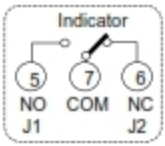
## FAILSAFE



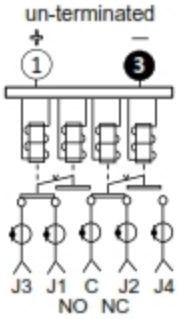




Fig. 1

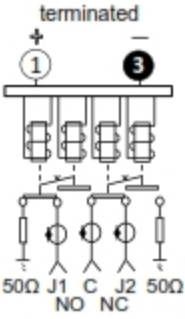



Fig. 2

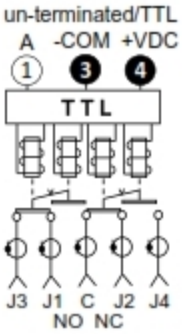



Fig. 3

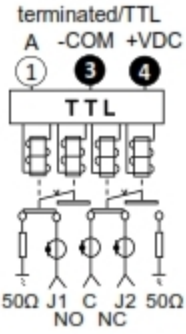
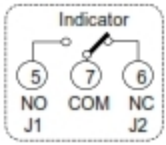



Fig. 4

## LATCHING



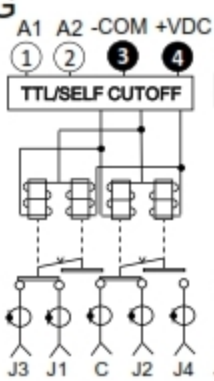




Fig. 5

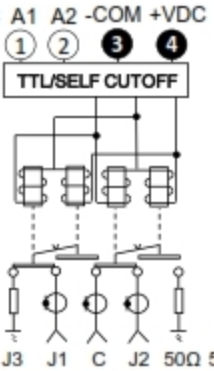



Fig. 6

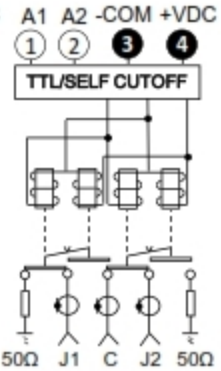



Fig. 7

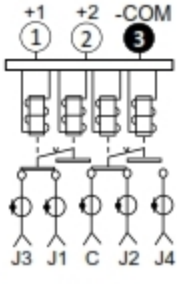



Fig. 8

## LOGIC TRUTH TABLE

FAILSAFE (Figs. 1 and 2)

| RF PATH | + | - |
|---|---|---|
| J1-C、J2-J4(T) | +VDC | GND |
| J2-C、J1-J3(T) | 0 | GND |

NOTE: +VDC=Positive rated voltage.

PULSE LATCHING (Fig. 8)

| RF PATH | +V1 | +V2 |
|---|---|---|
| J1-C、J2-J4(T) | +ΔV | 0 |
| J2-C、J1-J3(T) | 0 | +ΔV |

NOTE: +ΔV=Positive rated voltage pulse.

FAILSAFE TTL (Figs. 3 and 4)

| RF PATH | A |
|---|---|
| J1-C、J2-J4(T) | 1 |
| J2-C、J1-J3(T) | 0 |

LATCHING TTL/SELF CUTOFF (Figs. 5-7)

| RF PATH | A1 | A2 |
|---|---|---|
| J1-C、J2-J4(T) | 1 | 0 |
| J2-C、J1-J3(T) | 0 | 1 |

NOTE: +ΔV=Positive rated voltage pulse.

NOTE: (1) TTL logic: low "0" = 0.0V – 0.8V; high "1" = 2.4V – 5.5V.
(2) "T"=50Ω termination.
(3) "NC"=Normally Closed; "NO"=Normally Open.
(4) Consult the factory for the positive COM option.