## with or without Terminations

## MC8, MC0, MCF, MCM (LATCHING)

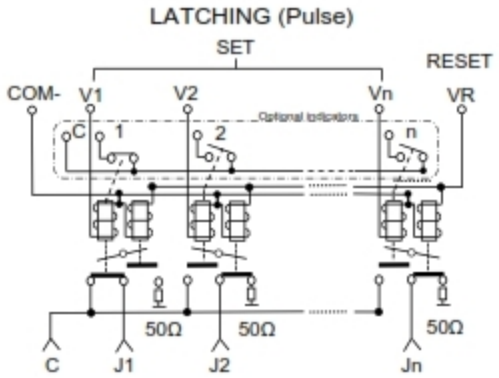


Fig. 1

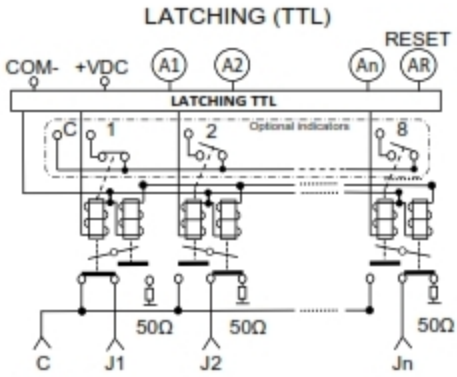


Fig. 2

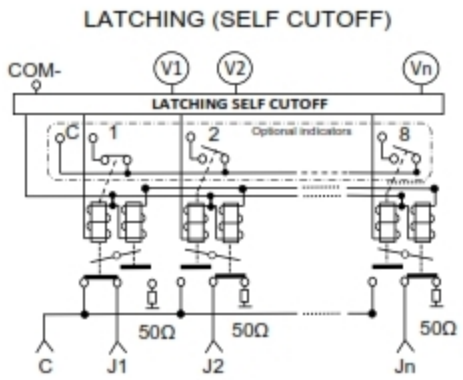


Fig. 3

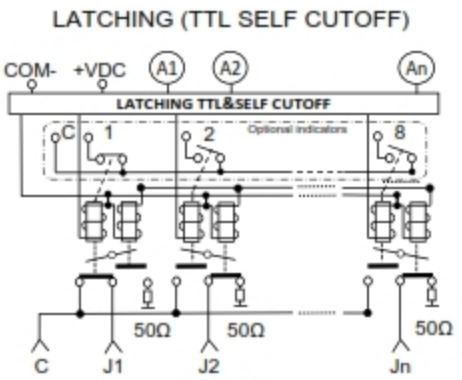


Fig. 4

## LOGIC TRUTH TABLE

LATCHING (Pulse) (Fig. 1)

| RF PATH | V(n) | VR |
|---|---|---|
| J(n)-C | +ΔV | GND |
| ALL J(n)-T or Open | GND | +ΔV |

LATCHING with TTL (Fig. 2)

| RF PATH | A(n) | AR |
|---|---|---|
| J(n)-C | 1 | 0 |
| ALL J(n)-T or Open | 0 | 1 |

LATCHING (SELF CUTOFF) (Fig. 3)

| RF PATH | V(n) |
|---|---|
| J(n)-C | +VDC |
| J(n)-T or Open | GND |

LATCHING with TTL & SELF CUTOFF (Fig. 4)

| RF PATH | A(n) |
|---|---|
| J(n)-C | 1 |
| J(n)-T or Open | 0 |

NOTE: (1) TTL logic input A(n): low "0" = 0.0V – 0.8V; high "1" = 2.4V – 5.5V.
(2) +VDC=Rated voltage; +ΔV=Pulse of rated voltage.